the entire thickness of the second wiring layer and at least part of the first wiring layer. The wiring layers have interconnect wire embedded therein.

Referring to Figure 1A of applicants' specification, there the applicants illustrate a portion of one integrated circuit (IC) 8. The IC 8 includes a semiconductor substrate 10, semiconductor devices 16, 18 located on the substrate 10, and a protective dielectric layer 14 covering both the semiconductor devices 16, 18 and the substrate 10. Exemplary semiconductor devices 16, 18 include transistors, diodes, and resistors. The IC 8 also includes multiple wiring layers 11-13 located on the layer 14, and an inter-wiring-layer capacitor 20 stacked over the protective layer 14. The inter-wiring-layer capacitor 20 extends through more than one of the wiring layers 12-13.

In claim 1, applicants recite an integrated circuit device "the charge-storage electrodes extending through the thickness of the second wiring layer and least part of the first wiring layer." (emphasis added). It is abundantly clear that this element of applicants' invention is not disclosed or described in the Roy reference. It is axiomatic that, to anticipate a claim, a reference must disclose every element of that claim. Nowhere in Roy is there suggested that the charge-storage electrodes extend through the thickness of the second wiring layer.

Referring to FIG. 1 in Roy, the capacitor is defined by the top electrode 16, the bottom electrode 12 and the dielectric 14. Clearly, the charge-storage electrodes of the capacitor described in Roy do not extend through the thickness of the dielectric layer.

Consequently, since Roy does not teach a capacitor with the features recited in claim 1, Roy does not anticipate applicants' claim 1. Furthermore, Roy does not render obvious applicants' invention. Specifically, Roy does not suggest to one skilled in the art to fabricate a capacitor in which the charge-storage electrodes extend through the thickness of one dielectric layer and into at least a portion of a second, adjacent dielectric. Nor does Roy provide any motivation to one skilled in the art to fabricate such a capacitor. Consequently, applicants submit that their claims 1, 1, 2 and 7 are patentable over Roy.

The Examiner rejected applicants' claims 1-4 as obvious under 35 USC § 103 (a). The Examiner cited US Patent No. 6,194,757 to Shinkawata (Shinkawata hereinafter) in view of US Patent No. 6,281,535 to Ma et al. (Ma et al. hereinafter) as the basis for his

rejection. Again, neither reference describes a capacitor in which the charge-storage electrodes extend through the thickness of one dielectric layer and into an adjacent dielectric layer.

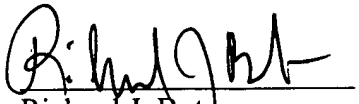
In Shinkawata, the upper and lower electrodes (24a and 27a, respectively, in FIG. 1) are clearly do not extend through the thickness of the dielectric layer 28. Similarly, in Ma et al., the electrodes 26 and 30 do not extend through the thickness of layer 38 and into an adjacent dielectric layer. Consequently, claims 1-4 are not obvious based on Shinkwata in view of Ma et al.

The Examiner rejected claim 5 as obvious under 35 USC SE 103(a). The Examiner based this rejection on Shinkwata in view of Ma et al. Claim 5 depends from claim 1. Consequently, claim is patentable over this combination of references for the same reason that claim 1 is patentable over this combination of references. Claims 6-8 are patentable over the cited combination of references for the same reasons.

In view of the foregoing arguments and amendments, applicants submit that their claims are in condition for allowance. Favorable action is respectfully requested.

Respectfully submitted,

Philip W. Diodato
Chun-Ting Liu
Ruichen Liu



Richard J. Botos
Reg. No. 32,016
(908) 582-3809

Date 4-16-02

Agere Systems Inc.
P.O. Box 614
Berkeley Heights, NJ 07922-0614